REMARKS

Examiner O. Nadav is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 8, and 14 have been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-20 rejected under 35 U.S.C. 103(a) as unpatentable over Ker et al (U.S. Patent 6,011,681) in view of Chen et al (U.S. Patent 6,016,002) is requested based on the Amended Claims 1, 8, and 14, and the following remarks.

Applicant agrees with the Examiner that Ker et al teaches an ESD protection device. However, Applicant notes two key differences between Applicant's ESD protection device and that taught by Ker et al. First, Ker et al teaches (in Fig. 8) coupling the second voltage supply (VDD2) to both the P+ region in the N-Well AND to the N-well. In other words, the N-well region is tied directly to the second voltage supply (VDD2). By comparison, Applicant only couples the P+ region 152 in the N-well 156 to the second supply (VCC2). The N-well 156 is not

tied to the second supply. Rather, the N-well 156 is left floating. This distinction is made clear by the device model in Fig. 7 where the N-well 312 is always at least a diode away from either of the supplies 324 and 328 or ground 320.

Second, Ker et al comprises a MOS gate within the N-well. This gate is between the P+ region within the N-well that is tied to VDD2 and a P+ region that rings the N-well. By comparison, the Applicant's device (Fig. 5) does not include any MOS gates. Applicant's device relies only on bipolar action to turn ON. Applicant's device has a different model of operation and does not require the additional process steps to form the MOS gates.

Further, the combination of Ker et al and Chan et al does not alter the above analysis. Chan et al teaches (Fig. 2) coupling the N-well 44 to the second supply (ANODE 50) and teaches the inclusion of an MOS gate 56 in the device. Therefore, Applicant believes that Ker et al and Chan et al also differ in these two, distinct ways.

To further clarify these differences, Applicant has amended Claims 1, 8, and 14. Amended Claims 1, 8, and 14 now include

the limiting language, "wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device." This language limits Applicant's device to a floating N-well where P+ region is coupled to the supply voltage by not the N-well. This language limits Applicant's device to not including a MOS-type gate either in the N-well or in the P-well. The above amendments are consistent with the original application (Fig. 5 and Specification pages 11-13) and do not represent new matters.

Applicant believes that the inclusion of the above amendments to Claims 1, 8, and 14 clarify the cited differences with the referenced art. Applicant therefore believes that Amended Claims 1, 8, and 14 are in condition for allowance. Further, dependent Claims 2-7, 9-13, and 15-20 represent patentably distinct further limitations on Amended Claims 1, 8, and 14 and, therefore, should be in condition for allowance.

Reconsideration of Claims 1-20 rejected under 35 U.S.C. 103(a) as unpatentable over Ker et al (U.S. Patent 6,011,681) in view of Chen et al (U.S. Patent 6,016,002) is requested based on the Amended Claims 1, 8, and 14, and the above remarks.

Reconsideration of Claims 1-20 rejected under 35 U.S.C. 103(a) as unpatentable over Chen et al (U.S. Patent 6,016,002) is requested based on the Amended Claims 1, 8, and 14, and the following remarks.

As discussed above, Applicant believes that Chen et al differs from the teaching of the Applicant in two ways. First, Chen et al couples the N-well to the second supply, while Applicant leaves the N-well floating. Second, Chen et al uses a MOS gate in the device, while Applicant does not use a MOS gate. Further, Applicant has clarified these differences by including further limitations in Amended Claims 1, 8, and 14. Therefore, Applicant believes that Amended Claims 1, 8, and 14 are in condition for allowance. Finally, dependent Claims 2-7, 9-13, and 15-20 represent patentably distinct further limitations on patentable subject matter and should, therefore, be in condition for allowance.

Reconsideration of Claims 1-20 rejected under 35 U.S.C. 103(a) as unpatentable over Chen et al (U.S. Patent 6,016,002) is requested based on the Amended Claims 1, 8, and 14, and the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner O. Nadav not find that the Claims are now Allowable that he call the undersigned at 989-686-3462 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

Please amend Claim 1 as follows:

1. (Amended) An electrostatic discharge protection device comprising:

a p-well region in a semiconductor substrate;

an n+ region in said p-well region wherein said n+ region is connected to a first voltage supply;

an n-well region in said p-well region wherein said n+ region is spaced from said n-well region a distance such that a depletion region extends therebetween during normal operation; and

a p+ region in said n-well region wherein said p+ region is connected to a second voltage supply of greater value than said first voltage supply during said normal operation wherein current is conducted through said n+ region to said p+ region during an electrostatic discharge event, wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device.

Please amend Claim 8 as follows:

8. (Amended) An electrostatic discharge protection device comprising:

a p-well region in a semiconductor substrate;

an n+ region in said p-well region wherein said n+ region is connected to a first voltage supply;

an n-well region in said p-well region wherein said n+ region is spaced from said n-well region a distance such that a depletion region extends therebetween during normal operation and wherein said distance between said n+ region and said n-well region is between about 0.2 microns and 1.0 microns; and

a p+ region in said n-well region wherein said p+ region is connected to a second voltage supply of greater value than said first voltage supply during said normal operation wherein current is conducted through said n+ region to said p+ region during an electrostatic discharge event, wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device.

Please amend Claim 14 as follows:

14. (Amended) An electrostatic discharge protection circuit on an integrated circuit device comprising:

a ground pad connected to an external ground reference and to a p+ region in a p-well in a substrate;

a first voltage supply pad connected to an external first voltage supply and to an n+ region in said p-well; and

a second voltage supply pad connected to an external second voltage supply of greater value than said external first voltage supply during normal operation and to a p+ region in an n-well region in said p-well region wherein said n+ region is spaced from said n-well region a distance such that a depletion region extends therebetween during said normal operation, [and] wherein current is conducted through said external second voltage supply pad to said external first voltage supply pad during an electrostatic discharge event, wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device.